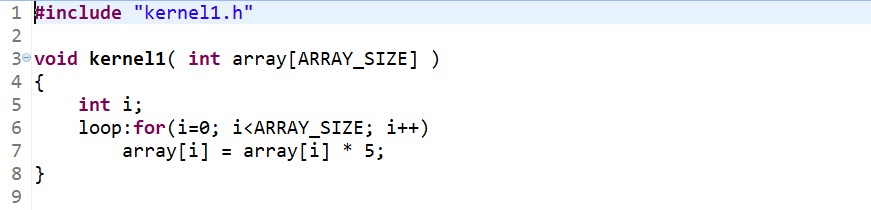
Homework 3 (Vivado HLS) Report

# Introduction

This report presents an overview on the design optimization of 8 loop kernels as a part of the Advanced Computer Architecture course (CS-470) at EPFL. It highlights the analysis of each kernel’s naïve implementation followed by the optimized implementation. The explanations and comparative results (in terms of area and timing) for all the optimizations are also presented. Please note that the results are given in terms of clock cycles assuming a clock period of 10ns.

# Kernel-1

The code for the loop kernel is shown below. The same code was used for the optimized version too.



## Optimization Steps

The naïve implementation does not give very good results (see table). The following observations and changes led to an optimized design:

1. The loop can be pipelined using the pipeline directive.
2. Each iteration is independent since it uses a different index i.
3. Hence, it was possible to achieve an iteration interval of 1.

## Synthesis Comparison

The synthesis reports for both the implementations can be compared in terms of timing and area:

**Performance Estimates:** The optimized version has the same iteration latency and trip count since the code was unchanged. However, the loop latency was halved because of pipelining, which led to an improvement in the total latency from 2049 to 1026 cycles.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Implementation** | **Total Latency** | | **Loop Latency** | | **Iteration Latency** | **Trip Count** | **Initiation Interval** |
| **Min** | **Max** | **Min** | **Max** |
| **Naïve** | 2049 | 2049 | 2048 | 2048 | 2 | 1024 | - |
| **Optimized** | 1026 | 1026 | 1024 | 1024 | 2 | 1024 | 1 |

**Utilization Estimates:** The optimized version uses 12 more LUTs but 8 less FFs when compared to the naïve version.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Implementation** | **BRAM\_18K** | | **DSP48E** | | **FF** | | **LUT** | | **URAM** | |
| **Unit** | **%** | **Unit** | **%** | **Unit** | **%** | **Unit** | **%** | **Unit** | **%** |
| **Naïve** | 0 | 0 | 0 | 0 | 35 | ~0 | 115 | ~0 | 0 | 0 |
| **Optimized** | 0 | 0 | 0 | 0 | 27 | ~0 | 127 | ~0 | 0 | 0 |